J1041 U.S. PTO
11/28/01

11-30-01

4/Fee Letter
3/27/02
EB

J1036 U.S. PTO
09/996279
11/28/01

LERNER AND GREENBERG, P.A.
PATENT ATTORNEYS AND ATTORNEYS AT LAW
2445 Hollywood Boulevard
Hollywood, Florida 33020
Tel: (954) 925-1100
Fax: (954) 925-1101

PATENTUSA[SM]
www.patentusa.com
patents@patentusa.com

Mailing Address:
Post Office Box 2480
Hollywood, FL 33022-2480

New York Office
153 E 57th Street
Suite 15G
New York, NY 10022

Herbert L. Lerner (NY Bar)
Laurence A. Greenberg (FL Bar)

Werner H. Stemer (FL Bar), Senior Attorney

Ralph E. Locher (FL, IL, MO Bars)
Manfred Beck (US & German Pat. Agent)
Mark P. Weichselbaum (TN Bar)
Gregory L. Mayback (FL Bar)
Markus Nolff (FL Bar)
Loren Donald Pearson (FL Bar)
Otto S. Kauder (Reg. Pat. Agent)
Denise A. Lettau (DC Bar)

"Express Mail" mailing label number: EL080599546US
Date of Deposit November 28, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202.

Michael Burns
MICHAEL BURNS

Docket No.: L&L-I0178

Date: November 28, 2001

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : LOTHAR RISCH ET AL.

Title : DOUBLE GATE MOSFET TRANSISTOR AND METHD FOR THE PRODUCTION THEREOF

3 sheets of formal drawings.
The payment in the amount of $830.00 covering the filing fee.
PCT Cover Sheet WO 00/74143 A1.

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(f). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicants
LAG:cp

J1036 U.S. PTO 09/996279 11/28/01

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
7. Dezember 2000 (07.12.2000)

PCT

(10) Internationale Veröffentlichungsnummer
WO 00/74143 A1

(51) Internationale Patentklassifikation⁷: H01L 29/786, 21/336

(21) Internationales Aktenzeichen: PCT/DE00/01714

(22) Internationales Anmeldedatum: 26. Mai 2000 (26.05.2000)

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

(30) Angaben zur Priorität:
199 24 571.1 28. Mai 1999 (28.05.1999) DE

(71) Anmelder (*für alle Bestimmungsstaaten mit Ausnahme von US*): INFINEON TECHNOLOGIES AG [DE/DE]; St.-Martin-Str. 53, D-81541 München (DE).

(72) Erfinder; und

(75) Erfinder/Anmelder (*nur für US*): RÖSNER, Wolfgang [DE/DE]; Heinzelmännchenstr. 2, D-81739 München (DE). SCHULZ, Thomas [DE/DE]; Annette Kolb Anger 13/V, D-81737 München (DE). RISCH, Lothar [DE/DE]; Tizianstr. 27, D-85579 Neubiberg (DE).

(74) Gemeinsamer Vertreter: INFINEON TECHNOLOGIES AG; c/o Lambsdorff & Lange, Dingolfinger Strasse 6, 81673 München (DE).

(81) Bestimmungsstaaten (*national*): JP, KR, US.

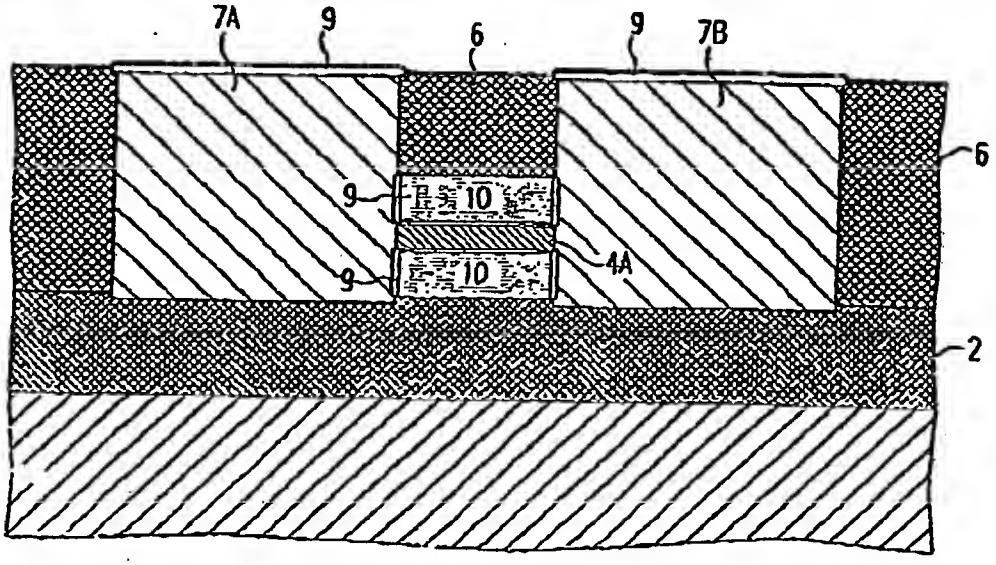
(84) Bestimmungsstaaten (*regional*): europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Veröffentlicht:
Mit internationalem Recherchenbericht.

[Fortsetzung auf der nächsten Seite]

(54) Title: DOUBLE GATE MOSFET TRANSISTOR AND METHOD FOR THE PRODUCTION THEREOF

(54) Bezeichnung: DOPPEL-GATE-MOSFET-TRANSISTOR UND VERFAHREN ZU SEINER HERSTELLUNG



(57) Abstract: The invention relates to a double gate MOSFET transistor and to a method for the production thereof. According to the invention, a semiconductor layered structure (4A) f a transistor channel to be formed is embedded in a placeholder material (3, 5) and is contacted by source (7A) and drain regions (7B) which are placed in recesses that are etched on opposing sides of the semiconductor layered structure (4A). In addition, the placeholder material (3, 5) is selectively etched out and is replaced by the electrically conductive gate electrode material (10).

[Fortsetzung auf der nächsten Seite]

WO 00/74143 A1